Energy-Efficient ARM64 Cluster with Cryptanalytic Applications

80 Cores That Do Not Cost You an ARM and a Leg

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 Thom Wiggers

iCIS | Digital Security
Radboud University

Outline

So you want to break crypto

1. Investigate attacks

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2. Implement attacks in software

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4. Profit

So you want to break crypto

1. Investigate attacks
2. Implement attacks in software
3. Run software on hugely expensive clusters
4. Profit

Typical Platforms

“Desktop” CPUs

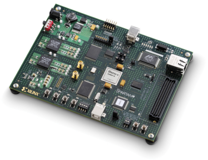
- Easy to program
- $$$$$
- Fairly high-power
- Fast with modern CPU extensions (SSE, AVX2)

GPUs

- Harder to program
- $$$$$
- Very high-power
- Much faster than CPUs on certain workloads

FPGAs

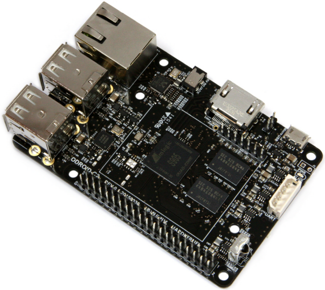
- Very hard to program
- $$$$$–$$$$$
- Low power
- Much, much faster than CPUs on certain workloads



Atypical platform

“Mobile” CPUs

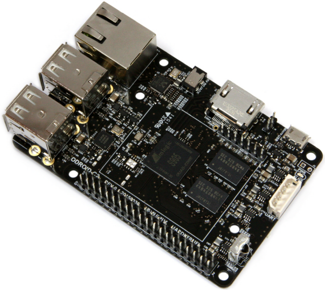
- Smartphones and IoT
- Easy to program for
- $$$$$
- Low power
- OK speeds?



ODROID-C2 devboard

ODROID-C2

- Cortex-A53 CPU
- 64-bit Quad-Core, 1536 MHz
- ARMv8
- 2 GiB RAM
- US$ 46



ODROID-C2 devboard

Shopping List

Item	Unit cost (USD)	Number	Total cost
ODROID-C2	$ 46	20	$ 920
5V Power Supply	$ 5	20	$ 100
Micro-SD cards	$ 17	20	$ 340
LAN cables	$ 1	21	$ 21
24-port switch (TL-SG1024D)	$ 85	1	$ 85
Total			$ 1466

Rack

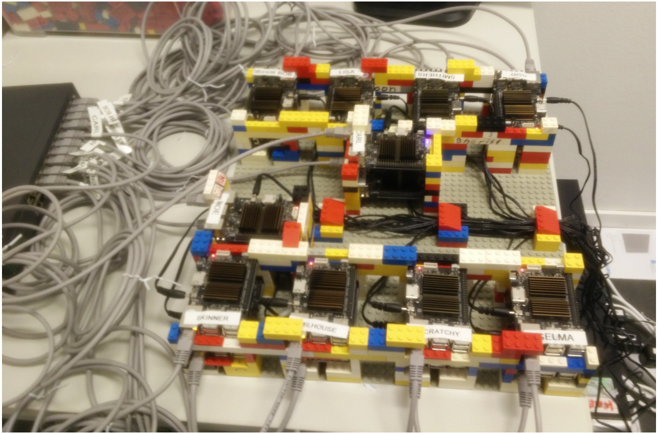


Figure: The assembled Lego “rack”. Cable management remains a subject for further investigation.

ECC2K-130

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- They describe highly optimised implementations, speeds and estimates for CPUs, PS3s, GPUs and FPGAs.
- To compare the ODROID-C2 to these platforms we should optimise ECC2K-130 for the Cortex-A53.

Cortex-A53 characteristics

- ARMv8-A architecture
- 32 registers
- ARM NEON extensions
  - 32 128-bit vector registers

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No detailed instruction characteristics are available

How to figure them out

- We have a cycle counter
- Idea: write small (micro) programs and measure how long they take (benchmarking).

```
measure_load:
mrs x17, PMCCNTR_EL0   ; store cycle counter at x17
ldr q0, [x0]           ; load q0 from address x0
mrs x18, PMCCNTR_EL0   ; store cycle counter at x18
sub x0, x18, x17       ; cycles spent = x18 - x19
ret
```

Benchmark results

Table: Hypothesised 128-bit vector instruction characteristics on the Cortex-A53. Latencies are including the issue cycles. `ldr` and `ldp` can be paired with a single arithmetic instruction for free.

Instruction	Issue cycles	Latency (cycles)
Binary arithmetic (`eor, and`)	1	1
Addition (`add`)	1	2
Load (`ldr`)	2	3
Store (`str`)	1	—
Load pair (`ldp`)	4	3, 4
Store pair (`stp`)	2	—

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Execution Pipelines

```
ldr q0, [x0]
eor v1.16b, v1.16b, v1.16b
```

Instruction	Issue cycles	Latency (cycles)
Binary arithmetic (`eor, and`)	1	1
Load (`ldr`)	2	3

Bitslicing

$$
\begin{aligned}
a &= \begin{pmatrix} a_4 & a_3 & a_2 & a_1 & a_0 \end{pmatrix} \\
b &= \begin{pmatrix} b_4 & b_3 & b_2 & b_1 & b_0 \end{pmatrix} \\
c &= \begin{pmatrix} c_4 & c_3 & c_2 & c_1 & c_0 \end{pmatrix} \\
d &= \begin{pmatrix} d_4 & d_3 & d_2 & d_1 & d_0 \end{pmatrix} \\
&\vdots
\end{aligned}
$$

Bitslicing

$$\begin{pmatrix} a \\ b \\ c \\ d \\ \vdots \end{pmatrix} = \begin{pmatrix} a_4 \\ b_4 \\ c_4 \\ d_4 \\ \vdots \end{pmatrix} \begin{pmatrix} a_3 \\ b_3 \\ c_3 \\ d_3 \\ \vdots \end{pmatrix} \begin{pmatrix} a_2 \\ b_2 \\ c_2 \\ d_2 \\ \vdots \end{pmatrix} \begin{pmatrix} a_1 \\ b_1 \\ c_1 \\ d_1 \\ \vdots \end{pmatrix} \begin{pmatrix} a_0 \\ b_0 \\ c_0 \\ d_0 \\ \vdots \end{pmatrix}$$

Optimising n-bit binary polynomial multiplications

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  - Compute $C = A \cdot B$ as
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I used Schwabe and Hutter's approach [HS15] for scheduling this in an efficient way.

Energy Usage

Item		Watts
ODROID-C2	Idle CPU load	2.3 W 5.3 W
Switch		13 W
20 ODROID-C2s	Idle CPU load	47 W 108 W
Complete System	Idle CPU load	59 W 122 W

Platform comparison

Table: ECC2K-130 on various platforms [Bai+09; Ber+10; Bos+10; Fan+10]

Type	Instance	Iters/s ($\times 10^6$)	Watts	Watts / (10^6 iters/s)
CPU	Core 2 QX6850	22.45	130 W	5.8
CPU	E5–2630L v4	61	55 W	0.9
GPU	GTX 295	63	289 W	4.6
PS3	Cell CPU	25.57	200 W	7.8
FPGA	Xilinx XC3S5000	111	5 W	0.045
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Cluster management software, benchmarking software and optimised multipliers available at thomwiggers.nl/research/armcluster/.

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Thank you for your attention.

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Elliptic-curve-discrete-logarithm Problem

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$$R_{i+1} = \sigma^j(R_i) + R_i,$$

   where $j = \mathrm{HW}((x_{R_i})/2 \mod 8) + 3$.
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3. Repeat until you get $R_i = a'P + b'Q = R_0$ with $b \neq b'$, $k = \frac{a'-a}{b'-b}$.

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For ECC2K-130 an expected $2^{60.9}$ iterations are needed [Bai+09].

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This gets us a $\Theta(K)$ speedup.

Number of operations per iteration

Iteration function
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HW is the Hamming Weight function and σ is the Frobenius endomorphism, so $\sigma^j((x, y)) = (x^{2^j}, y^{2^j})$.

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- In affine coordinates, this is one inversion, two multiplications, 21 squarings and seven additions over the field.
- Montgomery's trick [Mon87] allows, by batching up N inversions, to instead do $3N - 3$ more mults and only 1 inversion.

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